Design and Simulation of Folded-Cascode Amplifier

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ABSTRACT

This paper presents an amplifier design. Amplifier plays a vital role in the electronic manufacturing industry. There are many types of amplifiers with different specifications and design constraints. Differential amplifiers are the crucial devices for the power microelectronics design devices. These devices are used to maintain the gain and phase margin of the design. There are many amplifiers which are used to manufacture the electronic devices the folded cascode is one of them. Having higher gain and higher phase margin would keep the device stable. However, to design the folded cascode error amplifier to maintain the higher gain is used rather than telescopic topology. It is specially used in Power electronics such as DC to DC convertors and regulators devices. The designed folded cascode amplifier has an 83 DC gain and Phase Margin of 81 degrees with GBW of 119.86KHz. The Huge gain preserves the stability of the design in any devices. Large gain and phase keep the amplifier in saturation region and maintains the efficiency of the system. Significantly, phase margin keeps the error amplifier's loop stable. This design is used with a huge gain in many applications designing electronics devices. The biasing current is used to maintain the DC gain of the Error amplifier which is as low as 1µA.

Keywords: Folded cascode, Phase margin, open loop DC gain, Saturation

1. INTRODUCTION:

Designing of the folded cascode amplifier requires high performance for the design significance. CMOS technology is widely used in the electronics manufacturing industries. This design based on the CMOS technology *[1],[2]*. The elements like transistors are used in the design such as normal and native transistors. The Cadence Spectre 180nm tool is used for simulation and designing the folded cascode amplifier. The analog signals are sensitives and requires amplification. The amplifier design requires many parameters consideration like gain, phase, and gain-bandwidth product. Analog designs are significantly acknowledged as a high noise design *[3]*. This folded cascode error amplifier has low enough noise. The efficient design of the amplifier is required for many electronic systems. Applications of the amplifiers are mostly considered in the designing of the electronics devices. The amplifiers are used in the portable applications.

2. ANALYSIS OF FOLDED CASCODE ERROR AMPLIFIER:

The error amplifier is used in many power management designs using high DD gain and high phase margin for the stability of the system. This amplifier design provides the high DC gain and gain-bandwidth product. Error amplifier maintains the open loop and stabilize the poles and zeros. The highlighted transistors are native transistors irrespective of normal transistors. Transistors remains in the region of the saturation and sustain the amplification. Table:1. shows the values of the transistors.

3. DC GAIN, PHASE MARGIN AND GBW:

The key parameters of the Folded Cascode amplifier are DC gain, PM, and Gain- Bandwidth Product. These parameters perform significant role in the designing amplifier for any application. Table:2. shows values of the design parameters of amplifier.

Table.1

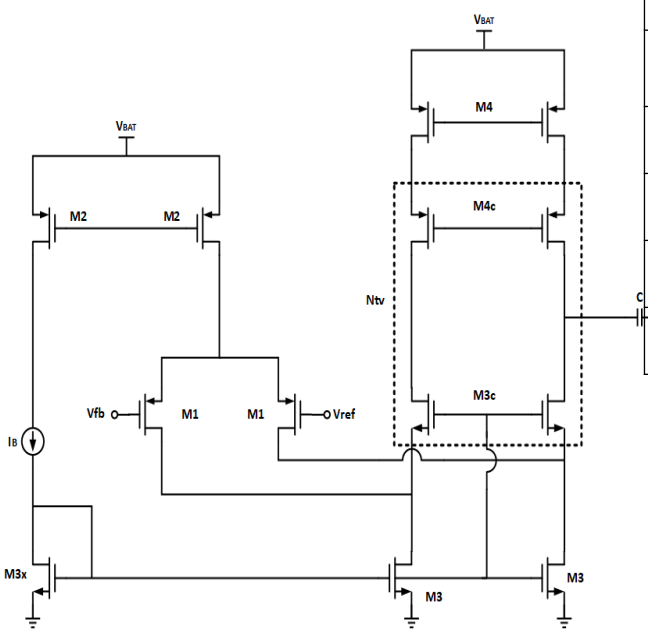

Table.2

Figure.1

4. RESULTS: A folded-cascode amplifier is designed for the power management applications. The amplifier can achieve open loop DC Gain of 83-dB and phase margin of 81 degree in Cadence Spectre. The plots of PM and DC gain are given in figure.2.

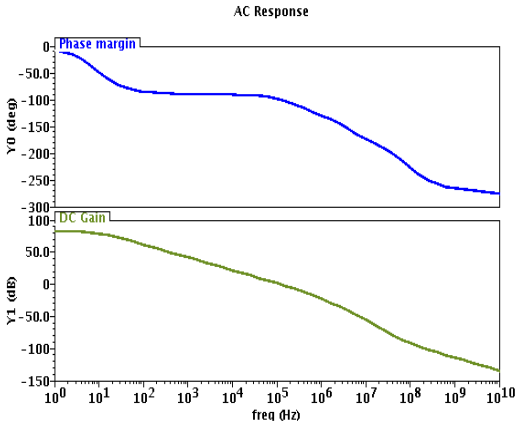

Figure 1: Phase Margin and DC gain

Parameter	Value
Vdd	2 V
I_B	1 uA
Dc gain	83 dB
PM	81 Degree
GBW	119.86 KHz
Cap	16 pF

(dB) of a Folded Cascode Amplifier

2. CONCLUSION:

: In this work, an operation of folded cascode amplifier is analyzed and simulated in 180nm CMOS technology. It is a fully differential folded cascode amplifier which is simulated with open loop DC gain of 83 dB and phase margin of 81 degree. The higher gain and bandwidth provide the stability of the Error amplifier. The GBW of the amplifier is 119.86 kHz with biasing current 1µA to maintain the DC gain.

3. REFERENCES

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